Register No.:

181

October 2023

Time – Three hours
(Maximum Marks: 100)

[N.B. 1. Answer all questions under Part-A. Each question carries 3 marks.

2. Answer all the questions either (A) or (B) in Part-B. Each question carries 14 marks.]

PART – A

1. Draw the NOR gate using CMOS.
2. What is design entry?
3. Write the general format for VHDL program.
4. Write the syntax for if else statement.
5. Draw the block diagram and write the truth table for 2 to 4 decoder.
6. Define de-multiplexer.
7. Draw the block diagram and write the truth table for JK flip-flop.
8. Draw the diagram for 3-bit down counter.
9. List out any three differences between PLA and PAL.
10. What are the types of ASIC?

[Turn over.....

PART – B

11. (a) Implement the function Y=AB+C using CMOS.

(Or)

(b) What are the different levels of abstractions in VLSI design? Explain.

12. (a) Write a VHDL code for logic gates OR, NOT.

(Or)

(b) Explain the different types of HDL modelling.

13. (a) Write a VHDL program for Half adder with diagram.

(Or)

(b) Write a VHDL program for 4 to 1 multiplexer with diagram.

14. (a) Write a VHDL program for D flip-flop with reset input and without reset input.

(Or)

(b) Explain 3-bit up counter with diagram.

15. (a) Draw the architecture of CPLD and explain.

(Or)

(b) Implement the function using $y=\sum 0,1,2,3,4,7$ using PAL.
